DEVICE FOR AUTOMATICALLY CONTROLLING A VOLTAGE APPLIED TO A DATA CONDUCTOR IN A SERIAL LINK

Field of the Invention

The present invention relates to a serial link cable between items of an electronic apparatus, and more particularly, to a universal serial bus (USB) connected to a voltage source for supplying power to an item of an electronic apparatus to which the cable is connected.

Background of the Invention

A universal serial bus (USB) type serial link for connecting two items A and B of an electronic apparatus, as illustrated in FIG. 1, includes four conductor wires 10, 12, 14 and 16. These four conductor wires are identified as follows. The first conductor wire 10 is for a ground connection, the second conductor wire 12 is for a data line referred to as DM or D-, and the third conductor wire 14 is for a data line referred to as DP or D+. The fourth conductor wire 16 is connected to a five-volt (5V) voltage supply referred to as V_{BUS}.

These conductor wires 10, 12, 14 and 16 are connected at each end to respective connectors 18 and 20 of the male type, for example, which cooperate with

female connectors 22 and 24 respectively attached to apparatus A and apparatus B. In this way, apparatus A can supply power to apparatus B with the voltage V_{BUS} by conductor wire 16.

Apparatus B includes a resistor Rr, referred to as a pull-up resistor, which connects conductor DP or DM to the power supply conductor. The value of this resistor Rr determines the communication speed (data rate) of apparatus B. Specifically, the communication speed is high if connected to DP or low if connected to DM.

Apparatus B comprises an internal power supply source, as shown by reference 26 symbolizing a voltage regulator for supplying a regulated voltage V_{CC} of 3.3 volts. The output terminal of this source 26 is connected to the pull-up resistor Rr. This power supply source 26 is derived either from the voltage V_{BUS} or from an external voltage V_{DD} at an input terminal 28.

The specifications of the USB require that the power supply source 26 for the pull-up resistor Rr be derived from or controlled by the power supply V_{BUS} such that when the voltage V_{BUS} is not present, the pull-up resistor does not supply a current to the data conductor DP or DM to which it is connected. This applies only to the items of apparatus B powered by V_{DD}, i.e., those that are not powered by V_{BUS}.

This specification results from the fact that the absence of V_{BUS} signifies that apparatus A is in a non-operating state (e.g., off) and, in that state, the voltage regulator 26 would supply a current to apparatus A which could risk damaging the latter. Accordingly, apparatus B must detect the presence of

V_{BUS} for supplying the pull-up resistor Rr only in the case where V_{BUS} is present.

Detection of V_{BUS} is obtained by a program of a microcontroller MC for apparatus B. The terminal V_{BUS} is connected to the input terminal of a Schmitt trigger type of electronic device 30 whose output terminal commands the state of a latch 32 belonging to a register 34, specifically with a 1 logic state for V_{BUS} present and a 0 logic state for V_{BUS} absent. In addition, the switching on or off of the regulator 26 is controlled by the state of a latch 36 belonging to a command register 38, specifically with a 1 logic state for the regulator in the OFF state and a 0 logic state for the regulator in the ON state.

The microcontroller program includes periodically reading the state of the state latch 32, and setting latch 36 to the 0 logic state (regulator 26 is ON) only in the case where latch 32 is in the 1 logic state (V_{BUS} is present).

When apparatus B is switched on, the regulator 26 must only be switched on in the presence of V_{BUS}. This is achieved by an initialization phase of the microcontroller in accordance with the flow chart of FIG. 2. After initialization of apparatus B, represented by operation 40, the microcontroller reads the latch 32. During the following operation 42, it compares the state of that latch with the 1 logic state. In the case of a positive comparison, it sets latch 36 to the 0 logic state (PDWN = 0) by operation 44, which concludes the initialization by the End state 46. In the case of a negative comparison, the microcontroller performs a new loop 48.

Once this initialization is carried out, the program 50 (FIG. 3) of the microcontroller MC periodically checks that the voltage V_{BUS} is present by reading the state of the latch 32 and comparing it, by operation 52, with the 1 logic state corresponding to the presence of V_{BUS}. In the case of a negative comparison, latch 36 is set to the 1 logic state (PDWN = 1) by operation 54, with the regulator 26 being switched off. In the case of a positive comparison, latch 36 is set to the 0 logic state by operation 56 (PDWN = 0), with the regulator 26 being maintained in the on state.

The above described approach satisfy the specification requirements for the USB, but consume microcontroller processing time since the state of the terminal V_{BUS} must be frequently checked.

Summary of the Invention

An object of the present invention is to provide an automatic monitoring of the input terminal V_{BUS} while avoiding the regular and frequent intervention of the microcontroller program.

The invention relates to a device for automatically controlling a voltage V_{cc} applied to one of two data conductors DP, DM of a USB type serial link cable in a peripheral apparatus B connected upstream to another apparatus A. The peripheral apparatus B comprises a supply voltage source which supplies the applied voltage V_{CC} to the data conductor DP or DM, and is susceptible of receiving on another conductor a supply voltage V_{BUS}.

The device includes a detection circuit for detecting the supply voltage V_{BUS}, and a memory circuit

for storing a state of the supply voltage V_{BUS}. A logic control circuit controls the supply source producing the voltage V_{CC} to set into operation the supply source only in the presence of the supply voltage V_{BUS}.

Brief Description of the Drawings

Other characteristics and advantages of the present invention shall become more apparent from the following description of a specific exemplary embodiment, the description being given in conjunction with the appended drawings in which:

FIG. 1 is a diagram showing a USB link between two items of electronic apparatus A and B according to the prior art;

FIGS. 2 and 3 are flow charts illustrating operation of a device according to the prior;

FIG. 4 is a logic truth table in accordance with the present invention;

FIG. 5 is a flow chart illustrating the automatic initialization phase of a device in accordance with the present invention;

FIG. 6 is an electronic circuit diagram showing the automatic device in accordance with the present invention;

FIG. 7 is a diagram illustrating the circuit for detecting the voltage V_{BUS} in accordance with the present invention; and

FIG. 8 is a flow chart illustrating the operation of the sate machine used in the detection circuit for detecting the voltage V_{BUS} in accordance with the present invention.

Detailed Description of the Preferred Embodiments

In the figures, like references designate like elements performing the same functions. FIGS. 1-3 illustrate the prior art which has been described above. The automatic device for controlling the regulator 26 comprises the following elements as best illustrated in FIG. 6. A detection circuit 60 detects the presence or absence of the voltage V_{BUS} on the corresponding terminal V_{BUS} of pin 24. A logic circuit 70 controls the regulator 26. A latch 36 controls register 38 of the microcontroller MC, and a latch 80 is for a state register 68 of the microcontroller MC. A latch 76 is for an interrupt state register 62 of the microcontroller MC, and a latch 78 is for an interrupt mask register (IMR) 64 of the microcontroller MC. The automatic device also includes an AND logic circuit 66.

The detection circuit 60, which shall be described in more detail below with reference to FIGS. 7 and 8, supplies a first signal set_vbusstat for setting the latch 80 to a 1 logic state when it detects a rising edge of the signal V_{BUS}, and a second signal reset_vbusstat for setting the latch 80 to a 0 logic state when it detects a falling edge of the signal V_{BUS}. The rising edge and the falling edge are those of the signal supplied by the circuit 30. The detection circuit 60 supplies a third signal set_vbusint which sets the latch 76 (ITVBUS) of the interrupt state register 62 (ISR) to a 1 logic state.

The logic circuit 70 comprises an inverter circuit 74 whose input terminal is connected to the output terminal of latch 80 of register 68 (SR). The latch 70 also comprises an inverting OR circuit 72 of which one of the two input terminals is connected to

the output terminal of the inverter circuit 74. The other input terminal is connected to the output terminal of latch 36 (PDWN) of control register 38 (CR). Latch 36 is set to a 0 logic state (PDWN = 0) during the initialization phase (FIG. 5) of the microcontroller MC, which signifies that the regulator 26 can be turned on.

This initialization phase (FIG. 5) comprises the start operation 90, the setting to a 0 logic state operation 92 and the end operation 94. In contrast with the prior art device, there is no loop 48 (FIG. 2). Latch 78 is set to a 1 or 0 logic state by the microcontroller MC to indicate whether or not it requires knowledge of latch 76.

The detection circuit 60 comprises (FIG. 7) a detection circuit 90 for detecting a rising edge and a falling edge of the signal supplied by the Schmitt trigger type of electronic device 30. The detection circuit 60 also comprises a state machine 92 and a counter 94. These different elements 90, 92 and 94 receive from the microcontroller MC a clock signal ck and a reset to zero signal nreset for producing the synchronization.

The detection circuit 90 further receives the signal $usbV_{bus}$ via circuit 30, and supplies the following three signals to the state machine 92. These signals are Vbus_rise corresponding to the detection of a rising edge, Vbus_fall corresponding to the detection of a falling edge, and Vbus_dd corresponding to the detection of a rising edge or a falling edge.

The detection circuit 90 receives from the state machine 92 a signal clr_event which indicates that the signal Vbus_rise or Vbus_fall has been

acknowledged and can be reset to zero. The detection circuit 92 supplies the three signals defined above: set_Vbusint, reset_vbusstat and set_vbusstat.

The counter 94 measures the time period which elapses after the detection of the rising edge or falling edge, starting from the appearance of a signal count_en corresponding to a change of state of the terminal V_{BUS}. When the counter has reached a certain predetermined value, this signifies that the change of state is stable and can be acknowledged by the state machine 92 which then receives the signal end_count.

The state machine 92 operates in accordance with the flow chart of FIG. 8. State 100 corresponds to a wait state of the machine. As soon as the detection circuit 90 supplies a signal Vbus_rise = 1 or Vbus_fall = 1, the state machine passes to a state 102 for resetting the different circuits to the 0 logic state.

In the case where the signal is Vbus_fall = 1, the machine passes to state 104 (Vbus_reset) which indicates an edge falling to the low level. If this low level is confirmed by the signal end_count = 1 of counter 94, the machine passes to the state 106 which supplies the output signal reset_vbusstat for setting the latch 80 of the state register 68 to a 0 logic state.

In the case of a signal Vbus_rise = 1, the machine passes to the state 108 (Vbus_set) which indicates an edge rising to the high level. If this high level is confirmed by the signal end_count = 1 of counter 94, the state machine passes to the state 110 that supplies the output signal set_vbusstat for

setting the latch 80 of the state register 68 to the 1 logic state.

In the two cases presented above, the state machine 92 passes from one of the states 106 and 110 to the state 112 which supplies the signal set_vbusint applied to the latch 76 of the interrupt state register 62. In these two cases, the state machine returns from the state 104 to the state 102 if the signal Vbus_dd = 1, i.e., if a signal Vbus_rise = 1 appears, and from the state 108 to the state 102 if the signal Vbus_dd = 0, i.e., if a signal Vbus_fall = 1 appears.

The logic circuit 70 provides the logic function defined by the truth table of FIG. 4 between the two binary variables determined by the states of the latches 80 and 36, i.e., the values of vbusstat and PDWN. This truth table shows that the regulator 26 is functioning only if the terminal V_{BUS} is powered by the USB connecting cable.